Abstract

Process and device for the verification of digital circuits

For the verification of digital circuits, which can have multiplier structures in particular, an equivalence test between the digital circuit (6) and a reference description (5) of this digital circuit is proposed, in such a way that firstly for the multiplier structures implemented in the digital circuit (6) the realized implementation alternative of several pre-defined different implementation alternatives (7) is determined in each case and inserted into the reference description (5) in place of the respective multiplication function, in order subsequently to execute the equivalence test with the reference description changed thereby. In this way, the structural equivalence between the reference description and the digital circuit to be verified can be substantially increased, which speeds up the verification process overall.